

MOSFET – N-Channel, Small Signal, SOT-23

60 V, 115 mA

2N7002L, 2V7002L

Features

- 2V Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable (2V7002L)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	60	Vdc
Drain–Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	60	Vdc
Drain Current	I_D	± 115	mAdc
– Continuous $T_C = 25^\circ\text{C}$ (Note 1)	I_D	± 75	
$T_C = 100^\circ\text{C}$ (Note 1)	I_{DM}	± 800	
– Pulsed (Note 2)			
Gate–Source Voltage	V_{GS}	± 20	Vdc
– Continuous	V_{GSM}	± 40	Vpk
– Non-repetitive ($t_p \leq 50\text{ }\mu\text{s}$)			

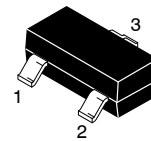
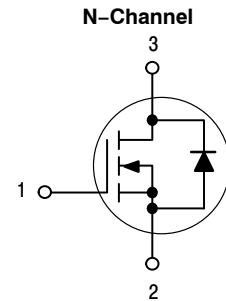
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR–5 Board (Note 3) $T_A = 25^\circ\text{C}$	P_D	225	mW
Derate above 25°C		1.8	mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation (Note 4) Alumina Substrate, $T_A = 25^\circ\text{C}$	P_D	300	mW
Derate above 25°C		2.4	mW/ $^\circ\text{C}$
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.
3. FR–5 = $1.0 \times 0.75 \times 0.062$ in.
4. Alumina = $0.4 \times 0.3 \times 0.025$ in 99.5% alumina.

$V_{(BR)DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
60 V	$7.5\text{ }\Omega$ @ 10 V, 500 mA	115 mA

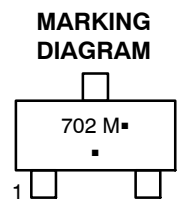


SOT-23
CASE 318
STYLE 21

702 = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.



ORDERING INFORMATION

Device	Package	Shipping†
2N7002LT1G	SOT-23 (Pb-Free)	3,000 Tape & Reel
2N7002LT3G		10,000 Tape & Reel
2N7002LT7G		3,500 Tape & Reel
2V7002LT1G	SOT-23 (Pb-Free)	3,000 Tape & Reel
2V7002LT3G		10,000 Tape & Reel
2N7002LT1H*		3,000 Tape & Reel
2N7002LT7H*		3,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Not for new design.

2N7002L, 2V7002L

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain–Source Breakdown Voltage ($V_{GS} = 0$, $I_D = 10\ \mu\text{Adc}$)	$V_{(BR)DSS}$	60	–	–	Vdc
Zero Gate Voltage Drain Current ($V_{GS} = 0$, $V_{DS} = 60\ \text{Vdc}$)	I_{DSS}	$T_J = 25^\circ\text{C}$	–	1.0	μAdc
		$T_J = 125^\circ\text{C}$	–	500	
Gate–Body Leakage Current, Forward ($V_{GS} = 20\ \text{Vdc}$)	I_{GSSF}	–	–	100	nAdc
Gate–Body Leakage Current, Reverse ($V_{GS} = -20\ \text{Vdc}$)	I_{GSSR}	–	–	-100	nAdc

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$)	$V_{GS(th)}$	1.0	–	2.5	Vdc
On–State Drain Current ($V_{DS} \geq 2.0\ V_{DS(on)}$, $V_{GS} = 10\ \text{Vdc}$)	$I_{D(on)}$	500	–	–	mA
Static Drain–Source On–State Voltage ($V_{GS} = 10\ \text{Vdc}$, $I_D = 500\ \text{mAdc}$) ($V_{GS} = 5.0\ \text{Vdc}$, $I_D = 50\ \text{mAdc}$)	$V_{DS(on)}$	–	–	3.75	Vdc
		–	–	0.375	
Static Drain–Source On–State Resistance ($V_{GS} = 10\ \text{V}$, $I_D = 500\ \text{mAdc}$) $T_C = 125^\circ\text{C}$ ($V_{GS} = 5.0\ \text{Vdc}$, $I_D = 50\ \text{mAdc}$) $T_C = 125^\circ\text{C}$	$r_{DS(on)}$	$T_C = 25^\circ\text{C}$	–	7.5	Ohms
			–	13.5	
		$T_C = 25^\circ\text{C}$	–	7.5	
			–	13.5	
Forward Transconductance ($V_{DS} \geq 2.0\ V_{DS(on)}$, $I_D = 200\ \text{mAdc}$)	g_{FS}	80	–	–	mS

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{iss}	–	–	50	pF
Output Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{oss}	–	–	25	pF
Reverse Transfer Capacitance ($V_{DS} = 25\ \text{Vdc}$, $V_{GS} = 0$, $f = 1.0\ \text{MHz}$)	C_{rss}	–	–	5.0	pF

SWITCHING CHARACTERISTICS (Note 5)

Turn–On Delay Time	$(V_{DD} = 25\ \text{Vdc}$, $I_D \cong 500\ \text{mAdc}$, $R_G = 25\ \Omega$, $R_L = 50\ \Omega$, $V_{gen} = 10\ \text{V}$)	$t_{d(on)}$	–	–	20	ns
Turn–Off Delay Time		$t_{d(off)}$	–	–	40	ns

BODY–DRAIN DIODE RATINGS

Diode Forward On–Voltage ($I_S = 115\ \text{mAdc}$, $V_{GS} = 0\ \text{V}$)	V_{SD}	–	–	-1.5	Vdc
Source Current Continuous (Body Diode)	I_S	–	–	-115	mAdc
Source Current Pulsed	I_{SM}	–	–	-800	mAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.



TYPICAL ELECTRICAL CHARACTERISTICS

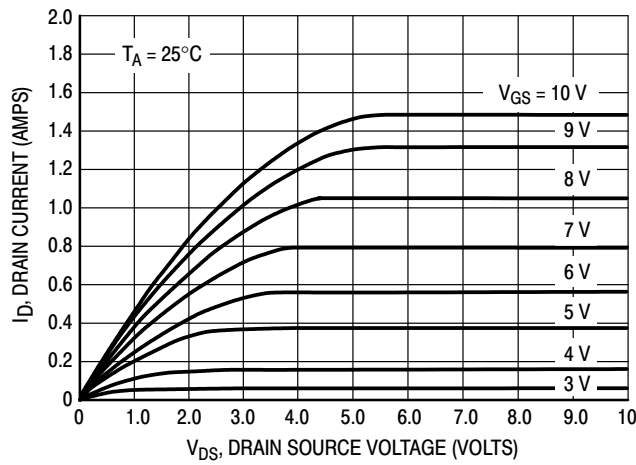


Figure 1. Ohmic Region

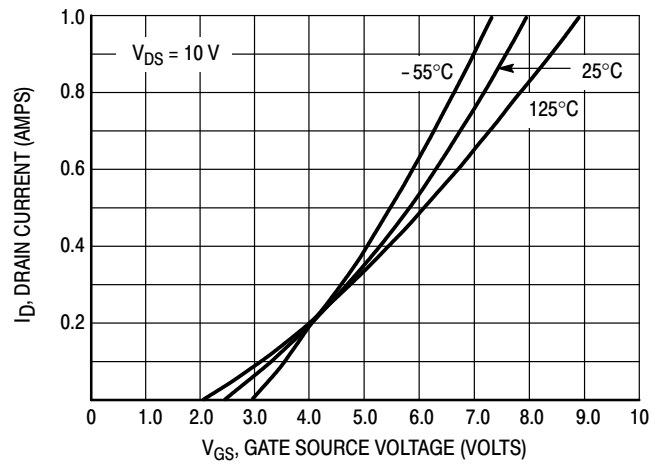


Figure 2. Transfer Characteristics

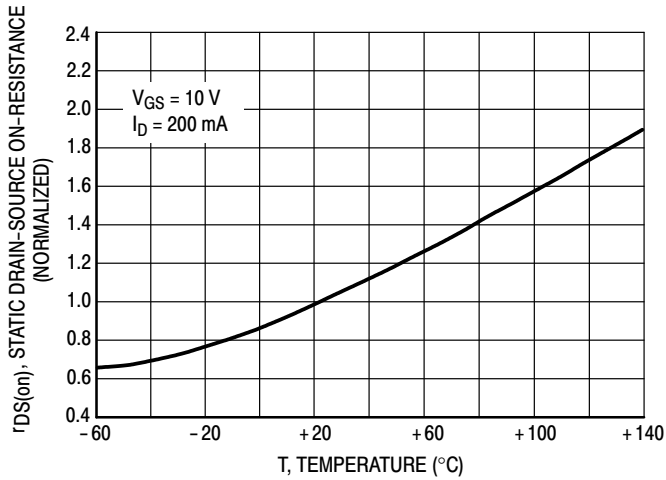


Figure 3. Temperature versus Static Drain-Source On-Resistance

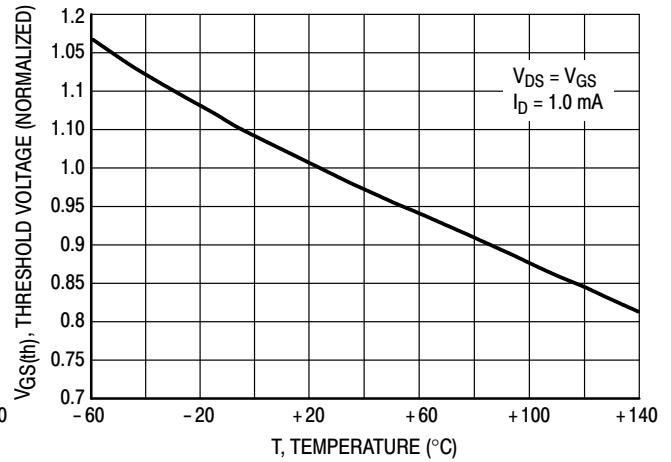
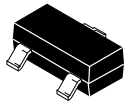


Figure 4. Temperature versus Gate Threshold Voltage

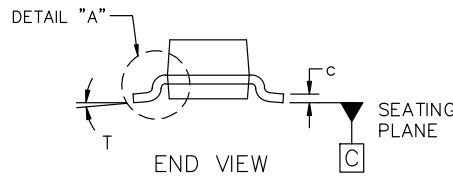
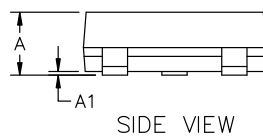
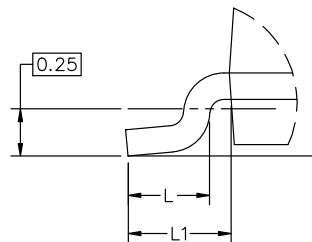
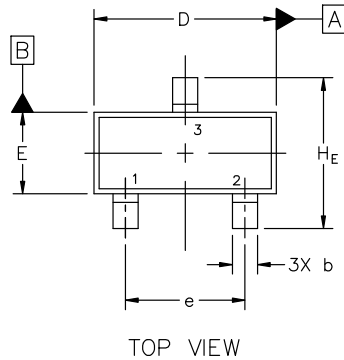


SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P

CASE 318
ISSUE AU

DATE 14 AUG 2024

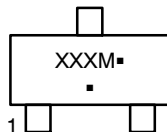


MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

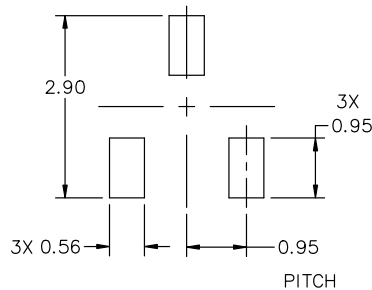
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23 (TO-236) 2.90x1.30x1.00 1.90P	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

DOCUMENT NUMBER:	98ASB42226B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOT-23 (TO-236) 2.90x1.30x1.00 1.90P	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales